**REMARKS**

This is intended as a full and complete response to the Office Action dated July 10, 2007, having a shortened statutory period for response set to expire on October 10, 2007. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-34 are pending in the application. Claims 1-16 and 18-34 remain pending following entry of this response. Claims 1, 16, 28, 31, and 34 have been amended. Claims 17 and 35 have been cancelled. Applicants submit that the amendments do not introduce new matter.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 16, 28, 31 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by *Owen et al.* (U.S. Patent No. 5,161,157, hereinafter "*Owen*").

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case, *Owen* does not disclose "each and every element as set forth in the claim". For example, regarding claim 1, *Owen* does not disclose replacing at least one of a row or column containing one or more defective storage cells with a redundant row or column, and thereafter replacing at least one word containing one or more defective storage cells with a redundant word without replacing the entire row containing the at least one word. *Owen* discloses replacing defective memory cells with available redundant memory cells. *See Owen*, Column 5: Lines 21-40. The defective memory cells may be faulty rows, words, bits, or columns. *See Owen* Column 5: Lines 46-51. However, *Owen* does not disclose a two stage process wherein, in a first stage, at least one of a row or column containing one or more defective storage cells is replaced with a redundant row or column, and in a second stage after the first stage, at least one word

containing one or more defective storage cells is replaced with a redundant word without replacing the entire row containing the at least one word.

Regarding claim 16, *Owen* does not disclose built-in self repair (BISR) circuitry configured to replace at least one of a row or column containing one or more defective storage cells with a redundant row or column and, after completion of the replacement of the at least one of a row or column by the redundant row or column, to replace at least one word containing one or more defective storage cells with a redundant word without replacing the entire row containing the at least one word. As discussed above, *Owen* simply replaces defective memory cells with redundant memory cells in a single stage. However, *Owen* does not disclose a two stage process for replacing defective memory cells.

The same reasons stated above apply to claim 34. That is, *Owen* does not disclose replacing at least one word with a redundant word after replacement of all rows or columns with redundant rows or columns. Furthermore, regarding claim 34, *Owen* does not disclose a plurality of memory built-in self repair circuits, each memory built-in self repair circuit being associated to one of the plurality of memories, wherein one block of redundant word elements is used for replacing words containing defective storage cells of the plurality of memories.

Regarding claim 28, *Owen* does not disclose a plurality of n fault count registers for storing during the test of columns a corresponding number of faults in each column having an address stored in a column address register.

Regarding claim 31, *Owen* does not disclose a plurality of n fault count registers for storing during the test of rows a corresponding number of faults in each row having an address stored in a row address register.

Therefore, claims 1, 16, 28, 31, 34, and the dependents therefrom are believed to be allowable, and allowance of the claims is respectfully requested.

## Claim Rejections - 35 U.S.C. § 103

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Oonk* (U.S. Patent No. 6,862,703) in view of *Deas* (U.S. Patent No. 6,065,090).

Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Oonk* in view of Applicants' admitted prior arts.

Claims 16-21, 23-25 and 27-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Schwartz* (U.S. Patent No. 6,795,942) in view of *Deas*

Claims 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Schwartz*.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the third criteria.

For example regarding claim 1, the combination of *Oonk* and *Deas* do not disclose a replacing at least one of a row or column containing one or more defective storage cells with a redundant row or column, and thereafter replacing at least one word containing one or more defective storage cells with a redundant word without replacing the entire row containing the at least one word. *Oonk* only discloses a one stage repair mechanism to replace a column/row. *Deas* also discloses only a one stage word replacement scheme. Therefore, the combination of *Oonk* and *Deas* do not disclose a two stage process for replacing defective memory cells as discussed in the previous section. Furthermore, because a two stage process is not disclosed, the combination of *Oonk* and *Deas* cannot, and does not, disclose a two stage process in the order that is claimed in claim 1.

Regarding claim 16, the combination of *Oonk* and Applicant admitted prior art does not disclose built-in self repair (BISR) circuitry configured to replace at least one of a row or column containing one or more defective storage cells with a redundant row or column and, after completion of the replacement of the at least one of a row or column by the redundant row or column, to replace at least one word containing one or more defective storage cells with a redundant word without replacing the entire row containing

the at least one word. As discussed above, *Oonk* does not disclose a two stage process for replacing defective memory cells.

Regarding claim 34, the combination of *Schwartz* and *Deas* does not disclose replacing of the at least one word with a redundant word is accomplished after replacement of all rows or columns with redundant rows or columns. *Schwartz* is directed to a one stage replacement mechanism to replace a column/row. *Deas* is also directed to a one stage word replacement scheme. Therefore, the combination of *Schwartz* and *Deas* do not disclose a two stage process for replacing defective memory cells. Furthermore, because a two stage process is not disclosed, the combination of *Schwartz* and *Deas* cannot, and does not, disclose a two stage process in the order that is claimed in claim 34.

Regarding claim 28, the combination of *Schwartz* and *Deas* does not disclose does not disclose a plurality of n fault count registers for storing during the test of columns a corresponding number of faults in each column having an address stored in a column address register.

Regarding claim 31, the combination of *Schwartz* and *Deas* does not disclose a plurality of n fault count registers for storing during the test of rows a corresponding number of faults in each row having an address stored in a row address register.

Therefore, claims 1, 16, 28, 31, 34, and the dependents therefrom are believed to be allowable, and allowance of the claims is respectfully requested.

## Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted, and
**S-signed pursuant to 37 CFR 1.4,**

/Gero G. McClellan, Reg. No. 44,227/

Gero G. McClellan
Registration No. 44,227
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicants